A $2\mu W$ Biomedical Frontend with $\Sigma\Delta$ ADC for Self-powered U-Healthcare Devices in $0.18\mu m$ CMOS Technology

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***Abstract*—This paper presents an ultra-low power analog front end (AFE) with $\Sigma\Delta$ modulator ADC meant for acquisition of biopotential signals. The system consists of a signal conditioning stage with programmable gain and bandwidth, a mixed signal automatic gain control (AGC), and a $\Sigma\Delta$ ADC. The full system is designed in UMC $0.18\mu m$ CMOS. The AFE achieves an overall linearity of more 10 bits with $0.47\mu W$ power consumption. The ADC provides 2^{nd} order noise shaping while using single integrator and an ENOB of $\sim$12 bits with $1.4\mu W$ power consumption. The system was successfully tested for a ECG signal from PTB database.**

I. Introduction

Cardiovascular diseases (CVDs) have been reported to cause most number of deaths globally [1]. This calls for a system which focuses not only on curing the illness (hospital-centric approach), but also on prevention and early detection of symptoms (patient-centric approach). Continuous ECG monitoring of biosignals become mandatory for such systems. All this, augmented with the radical advancement in CMOS and wireless communication technologies, has given impetus to concept of u-Health (ubiquitous healthcare) and use of wireless body area network (WBAN) based applications [2]-[4].

Hence, there is a growing need for acquisition systems with the following salient features (1) small size (2) light weight (3) portable (even wearable) (4) low voltage and low power consumption (to enhance battery life; self-powered systems are welcomed) (5) low input referred noise (6) tunable bandwidth (to cater multiple biopotential signals), and (7) programmable gain (to handle very weak signals and high dynamic range).

Lately there has been a spur in the number of research and publications related to self-powered acquisition systems for body sensor nodes (BSN). Incorporating energy harvesting mechanism can endow BSNs an indefinite lifetime. An ultra-low power system rendering the functionality of acquiring, processing and transmitting is presented in [5]. The BSN chip is powered by the energy harvested from human body heat through a thermoelectric generator (TEG). Another batteryless acquisition system powered by an adaptive RF scheme is reported in [6]. Reference [7] presents an excellent review on self-sustainable systems. Some related works make their system reconfigurable also. Such a system with different types of monitoring is described in [8].

The block diagram of the proposed ultra-low power system for acquisition and digitization is shown in Fig. 1. The prime features of the system are:

1) An ultra-low power two stage capacitive-coupled signal conditioning circuit (AFE). Apart from providing programmable amplification, it also includes tunable 2^{nd} order highpass and lowpass characteristics.
2) An efficient gain control (AGC) mechanism to maintain the input of the ADC to an optimum level (for which the ADC provides maximum SNR). In all of the acquisition schemes (even those where gain is controlled via DSP) reported till date, the ADC is kept continuously on. Hence, the present scheme is envisaged to consume lesser power than the conventional ones because
    a) ADC is turned on only after AGC has finished its job, and
    b) it avoids gain control through a DSP which is very power hungry [12].
3) A low power high resolution discrete-time (DT) $\Sigma\Delta$ ADC that achieves 2^{nd} order noise shaping while using a single integrator.
4) Seamless $\Sigma\Delta$ ADC resolution reconfigurability with minimal hardware and almost zero power overhead. This facilitates the digital circuit, following the $\Sigma\Delta$ ADC, to reduce its power consumption by opting to process low resolution data. The proposed $\Sigma\Delta$ ADC implementation aids area and power cost-efficient switching between the two modes vis-a-vis other ADC architectures e.g. SAR ADC, pipeline ADC, etc.

II. Transistor Level Implementation of Individual Blocks

A. Signal Conditioning Stage with Programmable Gain and Tunable Bandwidth

In this work, the signal conditioning stage is implemented as a two stage amplifier with capacitive feedback see Fig. 2. The heart of each of the stages is a fully differential recyclic folded cascode (RFC) OTA adopted from [14]-[16]. The RFC is used to double the transconductance under the same current consumption, hence improving the noise efficiency factor (NEF) by a factor of $\sqrt{2}$. Moreover, PMOS input pair is used to

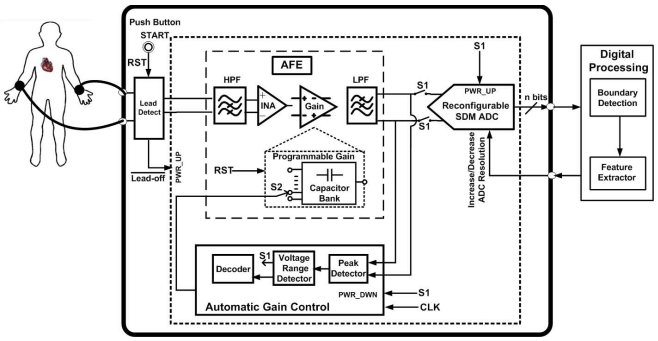

Fig. 1. Block diagram of the proposed acquisition system.

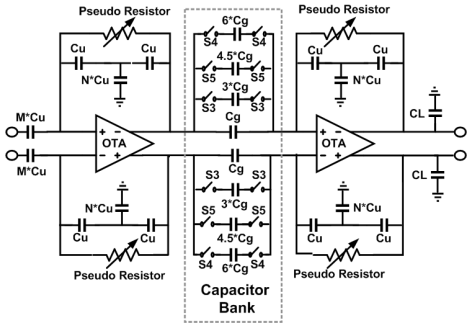

Fig. 2. Analog front-end providing both amplification and LPF and HPF characteristics. (M=10, N=8, C_U=1.03pF, C_g=103fF, and C_L=2-12pF). An input signal strength from 0.1mV to 1mV is considered here.

minimize flicker noise of the OTA. The input referred noise of the AFE can be decreased by increasing the transconductance of the input transistors. However in low power design, it is not plausible to boost the transcoductance by increasing the bias current. Fortunately the slewing requirements specified by the Association of Medical Instrumentation (AAMI) for biomedical applications are quite relaxed ($\sim$ 0.28V/s) [17]. Thus, bias currents as low as a few nanoamperes is enough to drive load capacitor in the order of tens of picofarad without slewing. All the transistors are operated in weak inversion to obtain such low drain currents. Operation in weak inversion provides other advantages too, viz., high current efficiency and high output voltage range.

The voltage gain of the closed loop amplifier is varied by changing the feedback factor. In order to set the DC common mode, a resistor is connected in parallel to the feedback capacitor as negative feedback. Coincidentally, this feedback resistor also determines the HPF cutoff frequency of the AFE, which is supposed to remove the low frequency noise and dc offset [18]. Realizing a pole $\sim$ 0.25Hz-1Hz, would require a very high resistance. Fortunately, this application does not need high accuracy in terms of high pass pole [19]. The high resistance value is obtained using a tunable pseudo-resistor [20].While the high pass cutoff frequency is varied by changing the gate voltage of the pseudo-resistor, the lowpass cut-off frequency is varied changing the load capacitance C_L. Further, a T-feedback network is used to reduce the effective feedback capacitance so that the same gain can be achieved with much smaller capacitance [21].

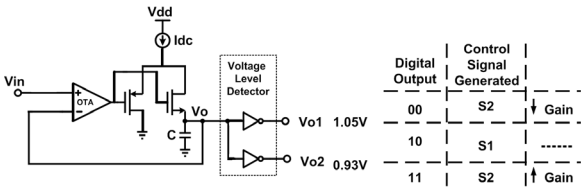

Fig. 3. Block diagram of the peak detector and voltage level detector. The digital output and the control signals generated are also shown. Here C=30pF and I_{dc}=92pA.

B. Automatic Gain Control

Gain of the system is controlled using a peak detector, digital control logic and a logic isolation block which decouples the gain control mechanism from the analog front end once the input falls in the desired amplitude range. Fig. 3 shows the scheme for peak and voltage level detection. The peak detector is adopted from [22]. The OTA of the peak detector is a low power folded cascode amplifier with all its transistors operating in weak inversion.

Also, the peak detector is designed such that it's total discharge time is higher than the time duration between two R peaks. Hence, here the discharge time is kept greater than 1s to prevent the digital control logic from varying the gain during low amplitude peaks(P,Q,T) of the ECG signal [23]. In the proposed circuit, the peak detector's output drops by only 22.5mV in half a second. A voltage range between 0.93V and 1.05V is determined to be the optimum input level for the $\Sigma\Delta$ ADC. Therefore, the inverters of the voltage level detector are sized such that the top inverter in Fig. 3 outputs a logical '1' only when it's input is lesser than 1.05V, while the other outputs a logical '1' only if it's input is lesser or equal to 0.93V. Therefore, the output of the level detector can be represented digitally as '00' '10' or '11' if its input is greater than, within or lesser than the desired level respectively. Finally, the subsequent digital logic is programmed such that it decreases (increases) the gain if the output of the level detector is '00' ('00'). It is designed so as to generate control signals, viz. S3, S4 and S5, which select the appropriate number of capacitors from the capacitor bank in the AFE (see Fig. 2). As soon as the level detector's output equals '10' a control signal S1(see Fig. 1) is generated which activates the path between AFE and ADC, turns the ADC *on*, and turns off the AGC.

C. Opamp-shared $\Sigma\Delta$ ADC

A conventional DT cascaded integrator feedback (CIFB) $\Sigma\Delta$ modulator with 2^{nd} order noise shaping is chosen for this work. Owing to the fact that the integrator is the most power hungry block of the $\Sigma\Delta$ ADC, twofold strategy was employed to minimize the ADCs power consumption. First, the whole ADC was designed for as minimum current as possible keeping the target SNR intact. Second, the 2^{nd} order noise shaping was achieved using only a single integrator, which reduces the power consumption to nearly half that of the ADC employing two integrators (see Fig. 4). The integrator is implemented using the enhanced recyclic folded cascode (ERFC) [14]-[16](see Fig. 5). The ERFC OTA has twice the bandwidth of a conventional folded cascode OTA for the same power and area.

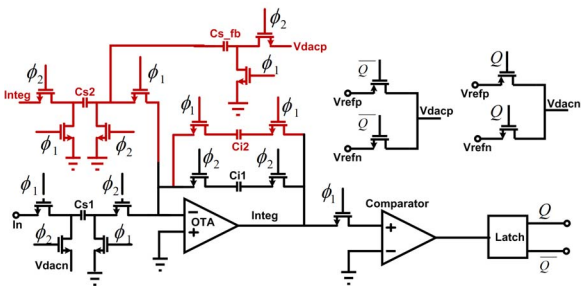

Fig. 4. Single ended representation of the fully differential opamp shared DT $\Sigma\Delta$ ADC . The circuit renders 1^{st} order noise shaping when only components in black color are activated, and 2^{nd} order noise shaping when the components in dark red are also activated. Here C_{S1}=0.67pF , C_{S2}=2.02pF, C_{S_fb}=0.79pF, C_{i1}=4pF, and V_{cm}= 0.9V. Here ϕ_1 and ϕ_2 are the two non-overlapping clock phases, V_{refp} and V_{refn} are positive and negative reference voltages , and, Q and $\overline{Q}$ are the ADC's output and it's compliment respectively.

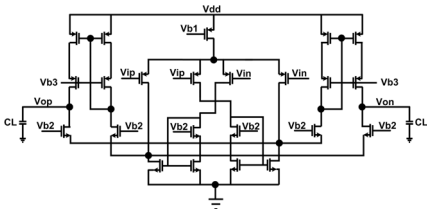

Fig. 5. Circuit diagram of an enhanced recyclic folded cascode opamp.

D. Seamless ADC Resolution Reconfigurability

The output of the $\Sigma\Delta$ ADC is taken up by the subsequent digital circuit for relevant signal processing like classification and feature extraction. Since the power consumed by this digital circuit is proportional to the resolution of the data it is processing, the digital circuit may opt to reduce its power consumption by reducing the resolution of the data it is processing. A control signal from the digital subsequent digital classification and feature extraction circuit selects the output resolution of the $\Sigma\Delta$ ADC. The proposed $\Sigma\Delta$ ADC is designed to work in two modes controlled by the digital block (1) the low resolution (6-8 bits), and (2) high resolution (10-12 bits) mode. In the first mode the $\Sigma\Delta$ modulator provides 1^{st} order noise shaping using one integrator. In the second mode the $\Sigma\Delta$ ADC modulator provides 2^{nd} order noise shaping, while using only a single integrator. Since integrators are the most power hungry circuit in the $\Sigma\Delta$ ADCs, here, a higher resolution is extracted keeping the power consumption nearly the same.

III. Results

The performance of the ERFC opamp, AFE and the ADC are tabulated in Table I, Table II and Table III respectively. The figure of merits are defined as in (1) and (2)

$$FOM1 = \frac{Power(W) * 10^{12}}{2^{\frac{SNR(dB)-1.76}{6.02}} * 2 * BW(Hz)} \; pJ/Conv. \quad (1)$$

$$FOM2 = DR(dB) + 10 * log_{10}(\frac{BW(Hz)}{POWER(W)}) \quad (2)$$

TABLE I. ERFC OTA Performance

Parameter	Value
Voltage Supply (V)	1.8
Current Consumption (μA)	0.67
Power Dissipation (μW)	1.116
DC Gain (dB)	94
CMRR (dB)	122
GBW (Hz)	15k
Slew Rate (V/ms)	66.5
Phase Margin (^{o})	74.73^o

TABLE II. AFE Performance

Parameter	Value			
	This work	[26]	[20]	[27]
Technology (μm)	0.18	0.35	0.35	0.18
Voltage Supply (V)	1.8	2.5	1	1
Power Consumption (μW)	0.47	0.62	0.9	0.8
CMRR (dB)	110	70	71.2	60
DC Gain (dB)	40-60	40.7	45.6-60	34
Bandwidth (Hz)	0.25-250	5m-200	4.5m-290	0.2-5.8k
NEF	4.4	1.96	3.26	2.79

TABLE III. Opamp Shared $\Sigma\Delta$ ADC Performance

Parameter	Value		
	This work	[24]	[25]
Technology (μm)	0.18	0.18	0.18
Voltage Supply (V)	1.8	0.9	0.7
Order	2^{nd}	2^{nd}	2^{nd}
Bandwidth (Hz)	150	10k	8k
Fs (MHz)	0.015	5	1.024
Power Consumption (μW)	1.4	200	80
Dynamic Range (dB)	76	83	75
FOM1 (pJ/Conv.)	0.905	0.866	1.087
FOM2	156.29	159.98	155

TABLE IV. Quality Assessment of the Reconstructed Signal

Parameter	Value
Percent Root Mean Square Difference (PRD)	19.4
Root Mean Square Error	0.0015
Signal to Noise Ratio (dB)	14.24
Maximum Amplitude Error (MAE)	2.93e-5
Cross Correlation (CC)	0.99
R-squared Score	0.96

Frequency response of the AFE is shown in Fig. 6. It evinces the utility of this system for the acquisition of various ExG signals. The plot for spectral density of the ADC's output is shown in Fig. 7. The figure clearly shows that the ADC renders 2^{nd} order noise shaping and SFDR of 70dB. The complete system was validated for a scaled ECG signal taken from the PTB database [28]. The digital output of the $\Sigma\Delta$ ADC (stream of 1s and 0s) generated by the Spectre simulator is exported to Matlab Simulink, where it is passed through a CIC filter to reconstruct the ECG signal. The quality assessment of the reconstructed signal wrt. the input ECG signal is tabulated in Table IV [30], [29]. As is shown in Fig. 6 the reconstructed waveform captures all the essential features of the ECG signal.

IV. Conclusion

An ultra-low power acquisition and digitization system is presented. While the AFE does the job of filtering and amplification, the $\Sigma\Delta$ modulator ADC digitizes the output. All the blocks are implemented in UMC $0.18\mu m$ CMOS technology. Each block is designed with minimum current consumption. Power dissipation is further saved by hardware sharing and keeping the ADC turned off during the initial phase of operation. All the blocks meet the desired expectations. The scheme is tested with a scaled version of the ECG

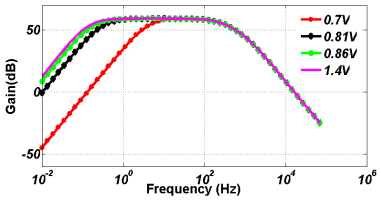

Fig. 6. Frequency response of the AFE. The high pass cut-off frequency is tuned by the gate potential V_{tune} of the pseudo-resistor. Different high pass cut-off frequency for different values of V_{tune} is shown.

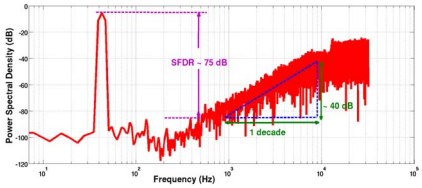

Fig. 7. PSD of the opamp shared $\Sigma\Delta$ ADC for an input of -5.2dB.

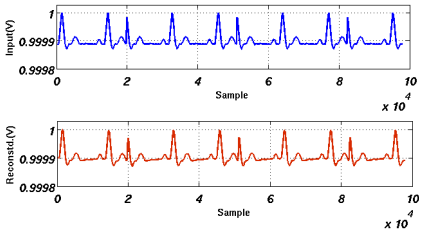

Fig. 8. The waveforms of the scaled input ECG signal taken from PTB database (top) and the output signal reconstructed using CIC filter(bottom).

signal taken from PTB database. The quality assessment of the reconstructed signal wrt. the input ECG signal reveals it's fidelity. The overall system consumes $\sim 2\mu W$ power. This system is useful for u-healthcare.

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