

# A Low Power Minimal Error IEEE 802.15.4 Transceiver for Heart Monitoring in IoT Applications

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**Abstract** With the advancement of communication technologies, the number of devices connected to the internet is increasing exponentially day by day. Multiple IoT applications have been evolved since recent past. Low power consumption, accuracy of transmission and robustness takes the center stage in developing these applications. IEEE 802.15.4 is a low power protocol for low range low data rate scenario. In this paper, we propose a minimal error modified IEEE 802.15.4 transceiver for IoT applications in health care. The health-care scenario, due to its critical nature, calls for an error free communication. We propose a modified frequency offset estimator which performs better in terms of error variance than the existing estimators for IEEE 802.15.4. The simulation result shows that the bit error rate and packet error rate performance of the proposed transceiver are significantly improved compared to the standard architecture. The proposed transceiver reduces the power consumption due to less number of retransmission per packet for successful transmission of the packet.

**Keywords** ZigBee · Low power transceiver · Differential encoding · Synchronization · Carrier offset · Heart monitoring application · ECG · Complex correlation · IEEE 802.15.4

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## 1 Introduction

Internet of Things (IoT) is gaining much attention since recent past due to the advancement of communication technologies. The number of devices connected to the internet are increasing exponentially nowadays. It is predicted that approximately 50 billion devices will be connected to the internet by 2020 [1]. Multiple IoT applications are being deployed such as smart health care, smart agriculture, smart cities, home automation, surveillance etc. Smart health care application belongs to a critical IoT application domain which includes several services like patient monitoring, remote assistance, telemedicine etc. [2]. Patient monitoring in health care applications includes transmission of medical data such as electrocardiogram (ECG), blood pressure, temperature etc. ECG is one of most important monitoring parameter which can be useful for patients to get immediate attention as well as for a healthy person to avoid any potential risk of any complications. In this work, we focus on communication of ECG data. However, the proposed method can also be used in any other applications which have data rate compatible to or lesser than ECG signal.

For any health care IoT application, the major concerns include low power consumption, robustness and accuracy of communications. We have taken these concerns into account while proposing the system. We utilize the IEEE 802.15.4 standard for communicating ECG data due its very low power consumption compared to other low range standards [3, 4]. As the maximum frequency in the ECG data can be 200 Hz, the minimum sampling rate requirement for data recovery is 400 samples per second. If the resolution of the data is maintained at 16 bits, then the minimum data rate of the ECG would be 6.4 Kbps, which makes it suitable for IEEE 802.15.4 transmission. Hence, the IEEE 802.15.4 standard can be adopted for ECG communication due to its low cost, low power consumption and reliable self-configurable capability which are the prime requirement of the ECG signal transmission.

Minimal Error requirement is another important factor in health care applications. For this purpose, we have proposed a modified IEEE 802.15.4 transceiver. We have proposed an ML frequency offset estimator which gives better error performance compared. The proposed method can significantly estimate the frequency offset up to 80 ppm. Since proposed transceiver gives better error performance, it provides more robustness against fading in the channel.

The rest of the paper is organized as follows. Section 2 describes the related works. The overall system model is described in Sect. 3. The complete description of the proposed transceiver is described in Sect. 4. Section 5 explains the results and performance analysis of the proposed system. The paper is concluded in Sect. 6.

## 2 Related Works

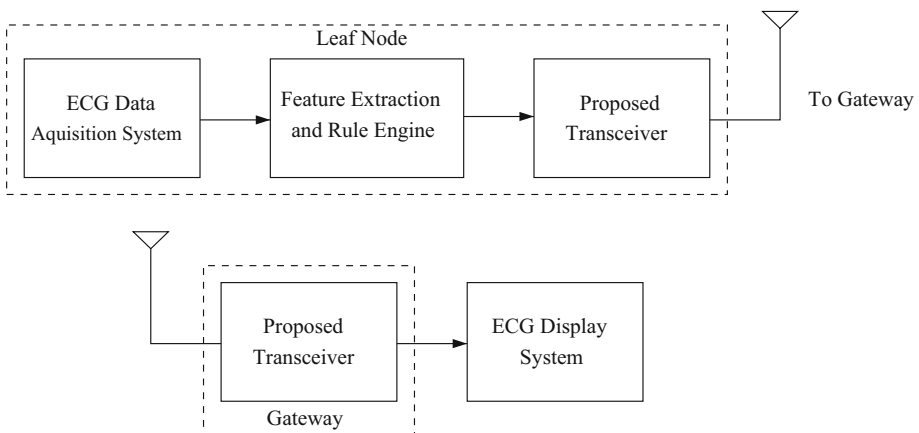
Multiple works have been proposed for providing communication in heart monitoring applications [5, 6]. ZigBee, Wi-Fi, and Bluetooth technologies have been used in the literature for wireless communication of ECG data. In [7], the Bluetooth module has been used as an intermediate node between ECG acquisition module and smart phone in ECG monitoring system. In [8] a Wi-Fi based system with a single-chip ECG acquisition module on Concerto MCU, a simplelink CC3000 Wi-Fi module and a smart phone was used. In [9], IEEE 802.15.4 module has been used to transmit ECG data. In [10], an ECG, EEG,

respiration rate and motion monitoring healthcare system was developed using IEEE 802.15.4 as communication standard. Since the data rate of ECG can be accommodated by the 802.15.4 specifications, In this work, we are utilizing a modified IEEE 802.15.4 standard due to its low power consumption. We propose a modified 802.15.4 transceiver which employs a differential encoding and proposed frequency offset estimator to provide minimal error in the ECG data.

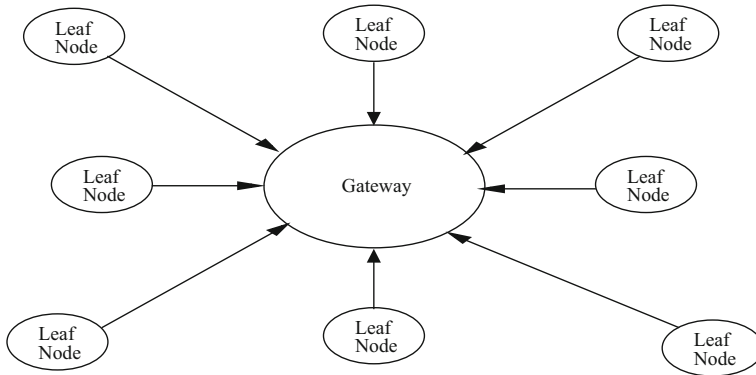
Synchronization is an essential task at the baseband receiver where synchronization includes finding of timing offset and matching of frequency and phase of the carrier signal to that of the transmitter side. If there is an offset in frequency and phase there will be the errors in demodulation. A significant amount of work is done in the field of carrier synchronization. In [11], data aided ML estimator for joint synchronization of frequency, phase and timing offsets is used. This work is done using a preamble sequence of alternating zeros and ones that are BPSK modulated. But in IEEE 802.15.4, the baseband receiver will receive a 256-bit spread sequence resulted from a 32 bit preamble of all zeros. Hence, the simplifications derived from an alternating zeroes and ones cannot be employed here. In [12], a simple and low complex frequency offset estimator using correlation for IEEE 802.15.4 receiver is proposed. But their estimator performance shows a significant gap between their error variance and Cramer Rao Lower Bound (CRB) for frequency estimators. In this paper, we propose a joint ML estimator for phase and frequency offset working on the spread sequence of the preamble. The performance of the proposed estimator is significantly closer to the CRB.

### 3 Overall System Architecture

The block diagram of complete heart monitoring system is depicted in Fig. 1. The ECG data is collected, processed and transmitted using the proposed IEEE 802.15.4 transceiver. For ECG data acquisition and processing, we have used adaptive rule engine based data acquisition system developed at IITH [13]. There is a wearable device on the patient side for this purpose. The transmitted ECG data from the device is collected at the nearest gateway which has the proposed transceiver. Multiple such devices called 'leaf node' can be connected to a single gateway in a star topology as shown in Fig. 2. In this way, multiple



**Fig. 1** Overall system architecture

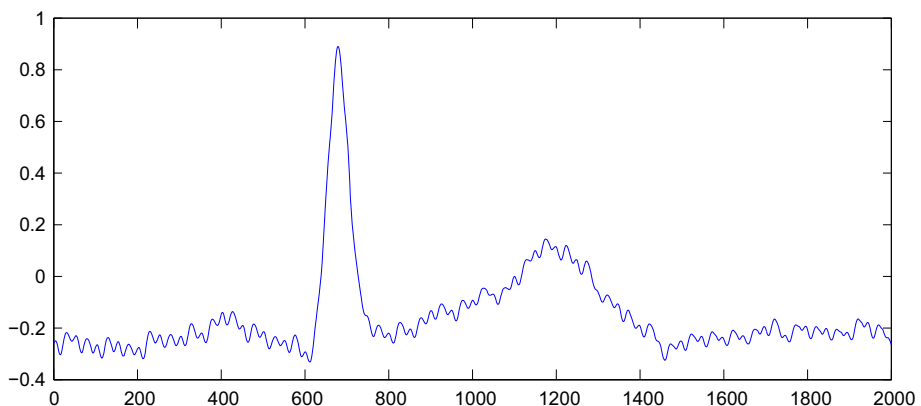


**Fig. 2** Topology of connecting leaf nodes to gateway

patients can be monitored using a single gateway. The final ECG waveform can be displayed at ECG display system which may be connected to the gateway through any other communication standard like cellular networks or WiFi etc. The doctor having access to display system can easily monitor and assist patients remotely using the proposed system. The working of each module in overall system architecture is discussed in the following subsections.

### 3.1 ECG Data Acquisition System

ECG conveys information about heart like heart rate and heart rhythm. All heart-related diseases like congestive heart failure, heart attack, and other diseases can be diagnosed by analyzing the changes in ECG pattern. The acquisition system is used to collect the ECG data (see Fig. 3) from the patient using signal processing techniques for removal of the noise generally generated from electrodes contact, body movements, and power line. Our data acquisition system has 3 lead ECG that requires 4 electrodes connected to the body. It contains several amplifying and filtering stages and it can be referred in [13] for a detailed description.



**Fig. 3** ECG signal collected by ECG data acquisition system

### 3.2 Feature Extraction and Rule Engine

ECG signal has few key features, the PR, QRS and ST intervals that convey critical information regarding the condition of the patient. The P wave gives information regarding the atrial contraction. The QRS interval represents the conductance and depolarization of the ventricles. The ST segment shows the time period in which the ventricles are iso-electric. The feature extraction section gives the important features (P, Q, R, S, T) of the ECG waveform. Figure 4 shows the features of the ECG waveform which is received by the ECG data acquisition system.

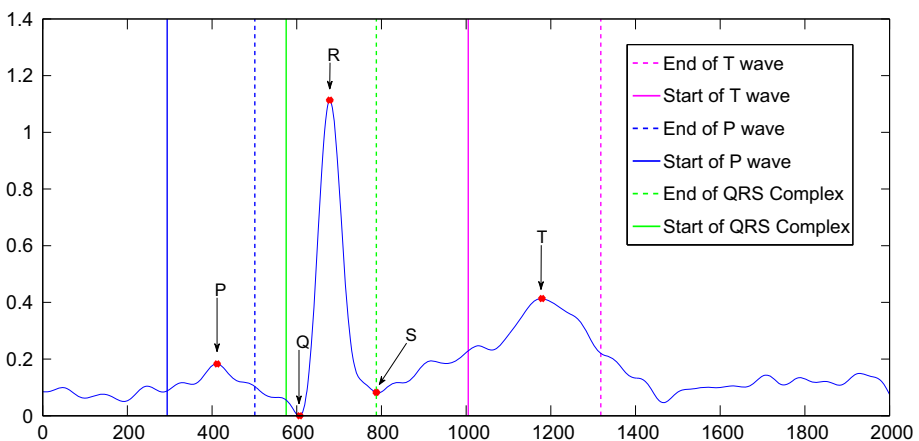
The extracted features are used to calculate the PR, QS and QT intervals in the rule engine section. The intervals calculated are then compared with a threshold limit and if it is detected as abnormal data if these intervals exceed the threshold. The detailed description of the feature extraction and the rule engine can be studied in [13]. The transmitter is activated in the case of abnormal data and the signal is transmitted to the gateway using the proposed IEEE 802.15.4 transceiver.

### 3.3 Proposed IEEE 802.15.4 Transceiver

The IEEE 802.15.4 standard is used for transmission of ECG data from the patient's wearable device to the gateway due to its simplicity, low cost, and low power consumption. We have proposed a modified 802.15.4 transceiver which gives better error performance and more robustness to frequency offset and fading channel. The proposed transceiver is discussed in detail in Sect. 3.

### 3.4 Gateway

Gateway receives the data from leaf nodes and transmits it to the ECG display system. It has the proposed transceiver for receiving the from the leaf nodes and has one more communication module like lte, wifi, cellular IoT etc. for transmitting data to ECG display system according to the application requirement. The multiple numbers of leaf nodes can



**Fig. 4** Extracted features P, Q, R, S, T from ECG data

be connected to the gateway and thus many patients can be monitored remotely by the doctor.

### 3.5 ECG Display System

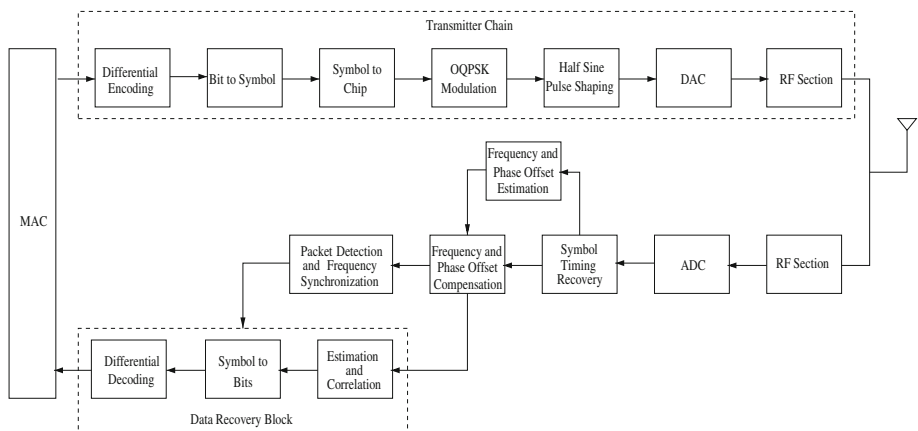
ECG display system gives the ECG information to the doctor in an optimum way. It displays the ECG waveform and gives the concluding result including ECG features. It is connected to the gateway using suitable communication standards such as internet, cellular network, NBIoT etc. Smart phone or computer can be used as ECG display system. The ECG display system can be directly also connected to gateway if remote motoring is not required. In this case, oscilloscope can also be used to display the ECG waveform.

## 4 Proposed Transceiver Architecture

The proposed transceiver is depicted in Fig. 5. The upper part of the block diagram shows the transmitter chain of the IEEE 802.15.4 while the lower part shows the receiver operating blocks. The transceiver switches between the transmitting and receiving mode according to MAC layer. At a time it works as a transmitter or as a receiver depending upon the command from the MAC layer. The MAC layer is responsible for feeding data to the transmitter chain and getting data from the receiver. Each part of the transceiver is described in the remaining part of this section. The transmitter chain is described first followed by the receiver blocks.

### 4.1 Transmitter Chain

The transmitter chain of the proposed transceiver is similar to standard 802.15.4 transceiver except the differential block encoding. The differential encoding is done to get benefit in frequency offset estimation and compensation. Using the differential encoding the bit error rate performance of the system improves which is discussed in the result section. The data coming from the MAC layer is first mapped to a frame according to 802.15.4 PHY layer frame format which is shown in Fig. 6. This is done by adding 32-bit



**Fig. 5** Block diagram of the proposed IEEE 802.15.4 transceiver

Preamble 32 bits	SFD 8 bits	Frame length 7 bits	Reserved bit 1 bit	PSDU (0-127) bytes
Synchronization Header		Physical layer Header		PHY Payload

**Fig. 6** IEEE 802.15.4 PHY packet format

preamble, 8-bit start frame delimiter (SFD) and length of the data in bytes. The preamble is a fixed bit pattern which helps in the estimation of frequency offset and identifying the valid 802.15.4 packet in the channel along with start of the payload.

the PHY layer frame bits are differentially encoded using equation as given below

$$y_k = x_k \oplus y_{k-1} \tag{1}$$

$y_0$  is taken as 0 at the start of the packet. The encoded bits which are at a rate of 250 Kbps are mapped to symbols in the bit-to-symbol block with each symbol equivalent to 4 bits. Each symbol is mapped to a fixed 32-bit chip sequence using direct sequence spread spectrum (DSSS). These chip sequences are inherently orthogonal to each other. The output of this symbol to chip block has a data rate of 2 Mbps. The signal is now modulated by using the Offset Quadrature Phase Shift Keying (OQPSK) modulation whose in-phase and out-phase component will be at a rate of 1 Mbps. Each component is passed through a half sine pulse shaping filter to limit the bandwidth of the signal. After the pulse shaping the signal is fed to DAC and then to RF section which transmits the signal in the channel as EM waves.

### 4.2 Symbol Time Recovery

Symbol time recovery blocks find the timing shift in the signal such that the samples can be selected at the peak of the pulse during decimation to minimize the demodulation error. We have used non-linear transformation based algorithm [14] for this purpose. The shifted pulse of  $L$  adjacent symbols are multiplied each other and then the timing error is estimated as the value of the shift at which the sum of the multiplication is found the maximum. After the calculation of the time shift  $\tau$ , the timing recovery block is bypassed and the required samples (peak of the pulse) are fed to the successive blocks.

### 4.3 Carrier Frequency and Phase offset Estimation

The carrier frequency offset ( $f_d$ ) and phase offset ( $\theta$ ) are manifested in the received baseband signal ( $z(t)$ ) as:

$$z(t) = s(t)exp(j(2\pi f_d t + \theta)) + n(t) \tag{2}$$

where  $s(t)$  : Modulated signal,  $s(t) = \sum_i c_i g(t - iT_c)$ ,  $c_i$  is a complex symbol and  $g(t)$  is the half sine pulse shape,  $T_c$  is the symbol period after DSSS,  $n(t)$  : Gaussian Noise with zero mean and variance  $\sigma_n^2$ .

The preamble used in IEEE 802.15.4 standard contains 32 bits of zeros that corresponds to eight symbols of the integer value 0. These eight symbols each have fixed 32 bit spread sequence of [11011001110000110101001000101110]. This gives a spreaded sequence of length 256 bits that maps to 128 OQPSK symbols. This fixed sequence helps in data aided

synchronization. The ML estimation uses the modulated signal  $s(t)$  derived from these known sequences.

The log likelihood function for the unknown carrier offset as given in [15] is:

$$\Lambda_l(\tilde{f}_d, \tilde{\theta}) = Re \left\{ \left[ \int_{T_0} z(t) s^*(t : \tilde{f}_d, \tilde{\theta}) e^{-i(2\pi\tilde{f}_d t + \tilde{\theta})} dt \right] \right\} \tag{3}$$

$s(t)$  : Known modulated signal of the spread sequence of the preamble.  $z(t)$  : Received signal.  $\tilde{f}_d$  : Frequency offset estimate.  $\tilde{\theta}$  : Phase offset estimate. The discrete time equivalent of the Eq. (3) when sampled at  $t = kT_c/2N$ , that is at twice of the chip frequency is:

$$\Lambda_l(\tilde{\nu}, \tilde{\theta}) = Re \left\{ \left[ \sum_{k=0}^{N_0-1} z[k] s^*[k] e^{-i(\pi\tilde{\nu}k + \tilde{\theta})} \right] \right\} \tag{4}$$

where  $N_0$  is the number of times the sequence is sampled.  $k = 0, 1, 2, 3, \dots$   $\tilde{\nu} = \tilde{f}_d T_c / N_0$ , the normalized carrier frequency offset

Rearranging the Eq. (4) gives :

$$\Lambda_l(\tilde{\nu}, \tilde{\theta}) = Re \left\{ \left[ e^{-i\tilde{\theta}} \sum_{k=0}^{N_0-1} z[k] s^*[k] e^{-i(\pi\tilde{\nu}k)} \right] \right\} \tag{5}$$

Let us define

$$\Delta(\tilde{\nu}) = \sum_{k=0}^{N_0-1} z[k] s^*[k] e^{-i(\pi\tilde{\nu}k)} \tag{6}$$

Then Eq. (5) becomes

$$\Lambda_l(\tilde{\nu}, \tilde{\theta}) = Re \{ [e^{-i\tilde{\theta}} \Delta(\tilde{\nu})] \} \tag{7}$$

The value of  $\tilde{\theta}$  that maximizes the likelihood function is given as:

$$\tilde{\theta} = arg \{ \Delta(\tilde{\nu}) \} \tag{8}$$

Now, define  $q[k] = z[k] s^*[k]$

Equation (6) becomes

$$\Delta(\tilde{\nu}) = \sum_{k=0}^{N_0-1} q[k] e^{-i(\pi\tilde{\nu}k)} \tag{9}$$

As clearly seen, Eq. (9) takes the form of a Discrete Fourier Transform (DFT). The value of  $\tilde{\nu}$  can be derived from maximizing  $\Delta(\tilde{\nu})$  .

$$\tilde{\nu} = max \left\{ \sum_{k=0}^{N_0-1} q[k] e^{-i(\pi\tilde{\nu}k)} \right\} \tag{10}$$

The DFT can be performed efficiently using an N-point Fast Fourier Transform (FFT). The accuracy of the estimated value  $\tilde{\nu}$  depends on the resolution of the FFT performed. The signal  $q[k]$  is zero padded to perform high resolution FFT that generates accurate value of  $\tilde{\nu}$ .



### 4.4 Frequency Offset Compensation

After the estimation of frequency and phase offset ( $\tilde{\nu}$  and  $\tilde{\theta}$ ), the signal compensated according to the following equation

$$z_c(t) = z(t)exp(-j(2\pi\tilde{f}_d t + \tilde{\theta})) + n(t) \tag{11}$$

where  $z(t)$  is received signal expressed in Eq. 2.

$\tilde{f}_d t$  is estimated frequency offset and  $\tilde{\theta}$  is estimated phase offset the above equation can be expressed in digital form as below:

$$z_c(kT_s) = z(kT_s)exp(-j(2\pi k\tilde{f}_d T_s + \tilde{\theta})) + n(kT_s) \tag{12}$$

where  $T_s$  is time duration between samples and  $T_s = T_c/N_0$  :  $T_c$  is chip period and  $N_0$  is the number of samples per chip taken during pulse shaping

$\tilde{f}_d T_s = \tilde{\nu}$  which is estimated by the previous block.

In this way, the factor due to frequency and phase offset is canceled by the estimated frequency and phase offset. The output of the offset compensation block is given to the Correlation and Estimation block.

### 4.5 Packet Detection and Frame Synchronization

This block decides whether incoming data is a valid packet or no and if there is a valid packet in the channel then it detects the starting of the frame. for frame synchronization, it performs the correlation of reference preamble symbol with shifted versions of the incoming signal using sliding windowing. If it finds a peak of the correlation above a certain threshold, then it indicates a valid packet in the channel. In [16], authors have shown that differential encoding reduces the false and missing probabilities in Packet Detection for BPSK Signals. The authors in [17] have analyzed the packet detection with differential encoding for IEEE 802.15.4 and have shown that this method provides robust packet detection. Our method is base on differential encoding and reference correlation where differential encoded and the modulated preamble is used to perform the correlation with the incoming signal and to find the peak of the correlation. The location of the peak is used to calculate the starting of the preamble, thus starting of PPDU data in the frame. If the packet is detected, the *data recovery* module to activated to decode the frame (excluding preamble).

### 4.6 Correlation and Estimation Block

This block perform the correlation of the signal with the modulated reference ship sequences. Thus it performs despreading and demodulation at the same time. The working of this block can be explained with the help of following equations:

The baseband received signal passed through the channel can be expressed as:

$$z(i) = \sum_{\tau=0}^L h(\tau)s(i - \tau) + n(i) \tag{13}$$

where  $z(i)$  : Received Signal,  $s(i)$  : Modulated Signal,  $n(i)$  : Gaussian Noise with zero mean and variance  $\sigma_n^2$ ,  $h(\tau)$  :  $\tau$ -th coefficient of the channel

$$h(\tau) = a(\tau)e^{j\theta(\tau)}$$

The channel is a Complex Gaussian distribution whose amplitude and phase follows Rayleigh and Uniform distributions respectively with  $L + 1$  taps.

For the  $k$ -th received signal, the correlator output is

$$\begin{aligned}
 J_k(l) &= \sum_{n=0}^{15} |z(i)g^*(l,n)|^2 \\
 &= \sum_{n=0}^{15} |g^*(l,n) \sum_{\tau=0}^L h(\tau)s(i-\tau)|^2
 \end{aligned}
 \tag{14}$$

where  $g(l,n)$  is the  $n$ -th sample of the  $l$ -th symbol's complex half sine modulated signal. Since the Gaussian noise is independent of the modulated signal, the correlation between noise and the modulated signal goes to zero. The expectation of the output gives

$$E\{J_k(l)\} = \begin{cases} 16\sigma_g^2 \sum_{\tau=0}^L |h(\tau)|^2, n = i - \tau \\ 16\sigma_{xy}^2 \sum_{\tau=0}^L |h(\tau)|^2, n \neq i - \tau \end{cases}
 \tag{15}$$

where,

$$\begin{aligned}
 \sigma_g^2 &= E\{|g(l,n)|^2\}, l = k \\
 \sigma_{xy}^2 &= E\{g^*(l,n)g(k,n)\}, l \neq k
 \end{aligned}$$

The symbol can be hence estimated as:

$$\hat{l}_k = \underset{l}{\operatorname{argmax}} \{J_k(l)\}
 \tag{16}$$

that is, the reference signal that gives maximum correlation with the received signal in the symbol duration is the estimated symbol. The flow of the block is shown in Fig. 7.

### 4.7 Data Recovery Module

The data recovery module includes the *estimation and correlation* block, *symbol-to-bit* block and *differential decoding* block. The working of the *Estimation and correlation* block is explained in the previous section. It gives the symbols as the output where the symbol is detected as the corresponding symbol to the chip sequence with which the correlation is found the maximum. The *symbol-to-bit* block converts the symbols to bits

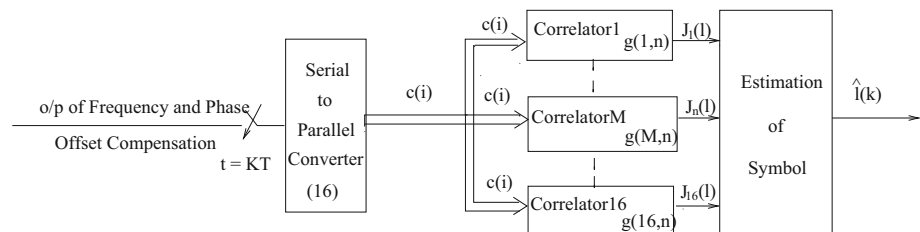


Fig. 7 Correlation and estimation block

and then bits are given to *differential decoding block*. The *differential decoding block* does the reverse operation of the differential encoding used in the transmitter chain. The output of this block is given to the MAC layer buffer where data is processed according to the requirement.

### 5 Performance Analysis

The analysis of the proposed architectures is done with the described ECG data acquisition system. The packet is constructed with 32-bits preamble and 80 bytes of payload coming from the ECG data acquisition system. The simulation is performed for 250,000 packets with SNR ranging from  $-10$  to  $30$  dB. The transmitted ECG signal and reconstructed ECG signal are shown in Fig. 8. We can observe that the proposed architecture faithfully recovers the ECG signal. The SNR is taken  $10$  dB for taking result in Fig. 8.

#### 5.1 Probability of False Alarm Analysis

The probability of miss and false alarm with differential encoded data for IEEE 802.15.4 was studied in [18]. It was proposed that differential encoded data performs better than the normal data. The variation probability of false alarm with SNR for both types of data for the proposed architecture is plotted in Fig. 9. It can be seen that the results for the normal data are as good as that of differentially encoded data. This is due to the better error management of the correlation and estimation block in the proposed architecture.

#### 5.2 Frequency Estimator Analysis

The Error variance [19, 20] of the proposed estimator is plotted in Eq. 10. The Cramer Rao Lower Bound (CRB) for the variance of a frequency offset estimator is given in [12] as

$$var(\delta f) = 3(2\pi^2 E_b/N_0 T_c^2 N(N^2 - 1))^{-1}$$

where  $N$  denotes sequence length,  $T_c$  denotes chip interval and  $E_b/N_0$  is SNR in linear scale.

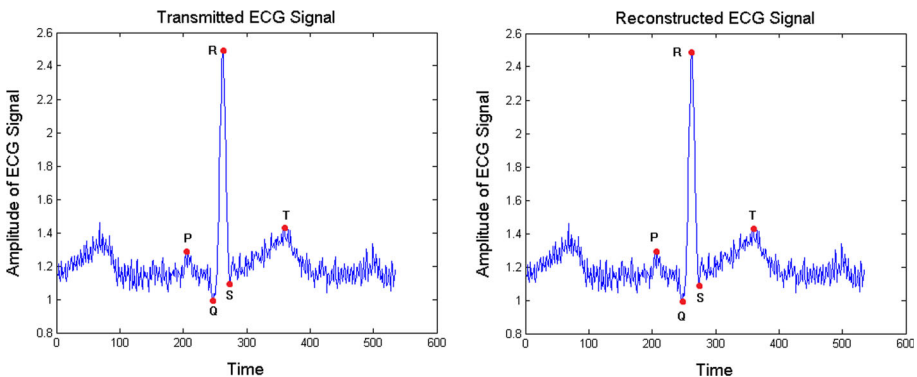
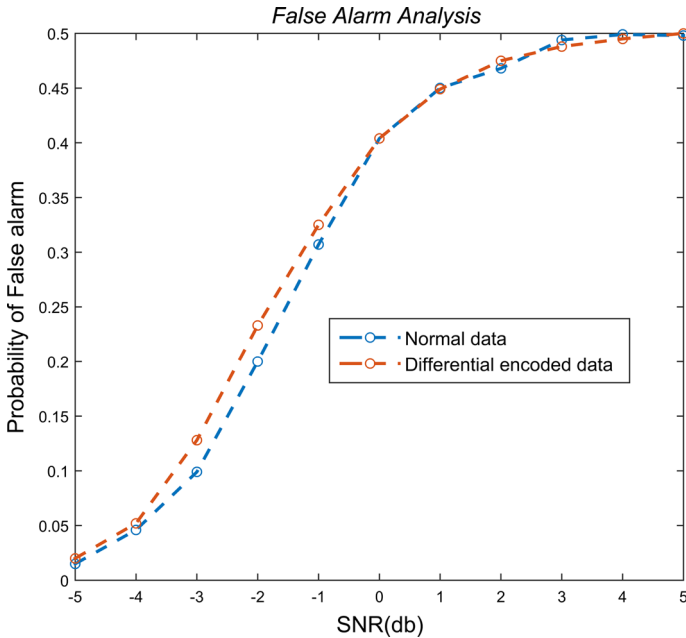


Fig. 8 Transmitted and received ECG signal



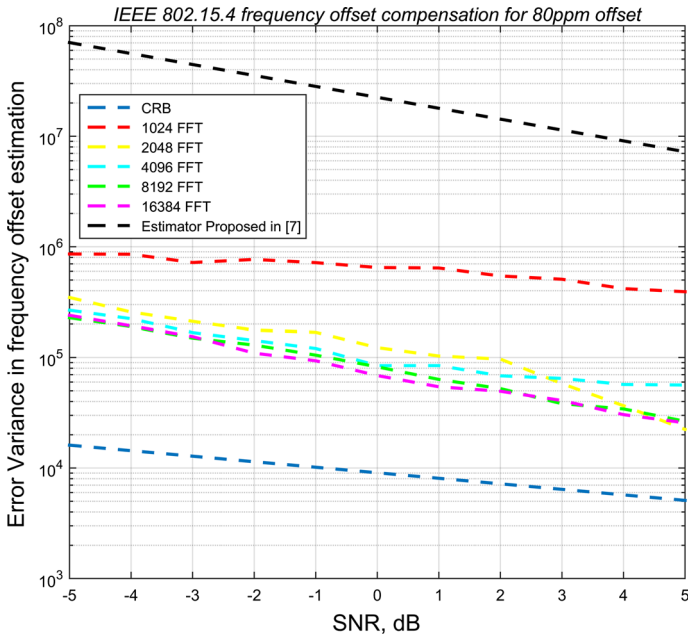
**Fig. 9** Comparison of probability of false alarm of the proposed transceiver with and without using differential encoding

The simulations have been performed by considering an offset of 80 ppm that is approximately 200 KHz which is the maximum offset in IEEE 802.15.4. As seen in Fig. 10, with the increase in FFT resolution, the error variance of the proposed estimator approaches the CRB. This is due to the increase in accuracy of the estimated value.

The scatters plot of the received packets are shown in Figs. 11 and 12. We can observe in Fig. 11, there cannot be an optimum decision boundary due to continuous rotation of the symbols. After passing through estimation and correlation block, the symbols can be easily detected Fig. 12.

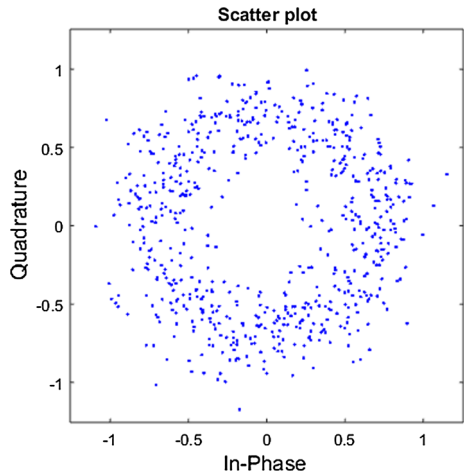
### 5.3 BER Analysis

The bit error rate of the transceiver is analyzed for different cases and the result is shown in Fig. 13. It has been analyzed without frequency offset compensation and with compensations under the various resolution of Fast Fourier Transforms (FFT) used in the estimator. It is observed that with the increase in the resolution the BER performance significantly improves. At 512 point FFT which is relatively less complex to design, the BER performance matches with the theoretical OQPSK–DSSS BER given in [21] at low SNRs. It can be seen that the estimator with 8192 points FFT has a gain of 2 dB at BER of 0.01 while 16,384 point FFT has more than 5 dB gain. This error performance is achieved due to complex correlation used for detection and accurate compensation for the frequency offsets. It is also observed that the frequency offsets, if not compensated degrades the performance severely. The frequency offset estimator improves the performance effectively even at the 80 ppm of frequency offset.



**Fig. 10** Analysis of error variance with different FFT resolutions and comparison with CRB for 80 ppm frequency offset

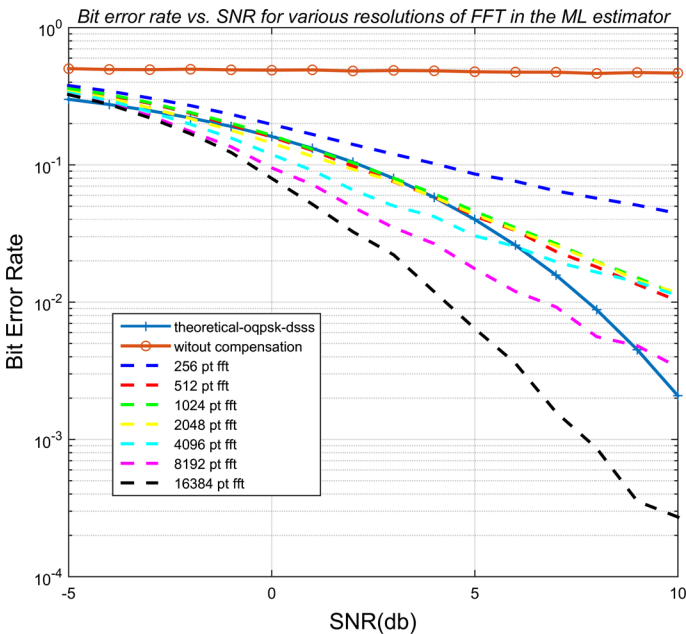
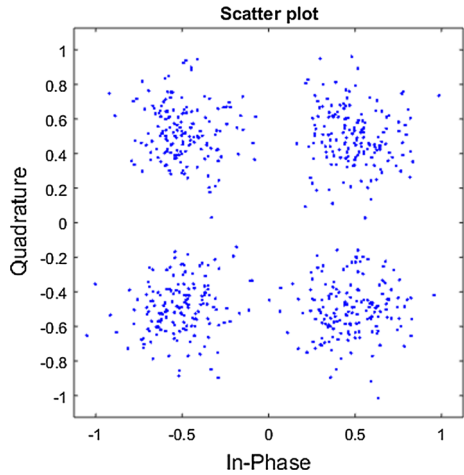
**Fig. 11** Constellation plot of received symbols without frequency offset compensation



### 5.4 PER Analysis

We have compared the packet error rate of the proposed transceiver with the standard receiver which consists Kay estimator [22] for frequency offset estimation. The PER curves of both the receivers are shown in the Fig. 14. The result shows that proposed transceiver performs better than the another one. We have taken the 30-byte packet size and have taken 25,000 iterations for the simulation.

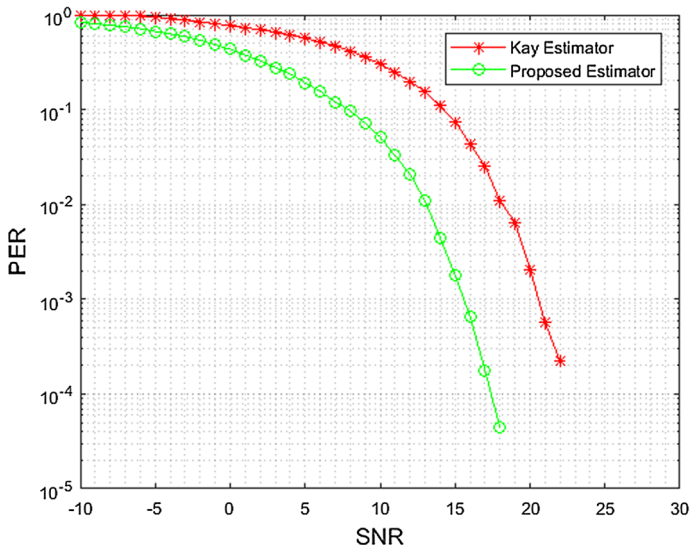
**Fig. 12** Constellation plot of received symbols with frequency offset compensation



**Fig. 13** Comparison of BER for different resolutions of FFT

### 5.5 Power Consumption Analysis

For power consumption analysis, we have considered a retransmission scenario in which packet will be kept on transmitting until successful transmission of the packet. Since the proposed transceiver offers better PER performance, the less number of retransmission will be there and hence the proposed transceiver will save the energy. We consider two nodes for comparison purposes: the first node  $N_1$  consist the proposed transceiver, whereas the



**Fig. 14** Comparison of PER between the proposed transceiver and the transceiver consisting KAY estimator

second node  $N_2$  has the standard transceiver which consists Kay estimator as frequency offset estimation. We assume that both nodes have the same central processing unit (CPU). Let  $P_1$  and  $P_2$  denote the power consumption by the the node  $N_2, N_2$  respectively. Let  $p_1, p_2$  be the probabilities of packet error rate respectively. Let  $r_1, r_2$  be the Estimated transmission per packet for a successful transmission.  $1 \geq r_1, r_2 < \inf$  as there will be at least one transmission per packet. The  $r_1$  and  $r_2$  can be calculated by the following equations

$$r_1 = \sum_{i=1}^{\infty} iP_1(i) \tag{17}$$

$$r_2 = \sum_{i=1}^{\infty} iP_2(i) \tag{18}$$

where  $P_1(i)$  and  $P_2(i)$  are the probabilities such that packet is transmitted on  $i^{th}$  attempt successfully while it has failed  $i - 1$  times. By replacing the values of  $P_1(i)$  and  $P_2(i)$ , the above equations can be simplified as follows:

$$r_1 = \sum_{i=1}^{\infty} ip_1^{i-1}(1 - p_1) = \frac{1}{(1 - p_1)} \tag{19}$$

$$r_2 = \sum_{i=1}^{\infty} ip_2^{i-1}(1 - p_2) = \frac{1}{(1 - p_2)} \tag{20}$$

Here we have considered a retransmission scenario in which packet will be kept on transmitted again until the successful transmission of the packet, Let the total estimated

**Table 1** Estimated transmission per packet with SNR

SNR dB	Proposed transceiver $N_1$		Node $N_2$		$\frac{E_1}{E_2}$
	PER ( $p_1$ )	ETP ( $r_1$ )	PER ( $p_2$ )	ETP ( $r_2$ )	
- 10	0.8341	6.0271	1	22.698	0.0003
- 5	0.6677	3.0095	0.9463	18.6202	0.1616
0	0.4329	1.7632	0.7724	4.3946	0.4012
5	0.1918	1.2373	0.5667	2.3081	0.5361
10	0.0514	1.0542	0.3033	1.4353	0.7345
15	0.0018	1.0018	0.0753	1.0815	0.9263
20	0	1	0.0021	1.0021	0.9979
25	0	1	0	1.0000	1.0000

energy consumption per packet be  $E_1$  and  $E_2$  for the node  $N_1$  and  $N_2$  respectively. This energy can be described by the following equations:

$$E_1 = r_1(P_1)T_1 \quad (21)$$

$$E_2 = r_2(P_2)T_2 \quad (22)$$

where  $T_1$  and  $T_2$  are the time taken for processing and transmission of a single packet. As we are using the same CPU on both the nodes, the processing time and energy consumed by CPU will be same on both the nodes. Moreover, we are not changing the RF sections of the transceiver which consume significant energy compared to digital baseband section [23]. We are only modifying frequency offset estimation block and estimation and correlation block. So, we can assume  $P_1 \approx P_2$ . We can further assume  $T_1 \approx T_2$ . This is due to fact that the processing time is same on both the nodes because both the nodes consist of the same CPU. Using these approximations in Eqs. 21 and 22, we can get the following

$$\frac{E_1}{E_2} = \frac{r_1}{r_2} \quad (23)$$

The values of  $\frac{E_1}{E_2}$  corresponding to  $p_1, p_2$  are given in Table 1 with different values of signal-to-noise ratio. We can observe that  $\frac{E_1}{E_2} < 1$  for all values of SNR. This indicates that energy consumption per successful packet transmission of proposed transceiver is always less than the standard one.

## 6 Conclusion

In this paper, we proposed a low power minimal error IEEE 802.15.4 transceiver and tested it for ECG data. The ECG signal from the data acquisition system is transmitted and faithfully reconstructed at the receiver. The proposed transceiver performs considerably better than the standard transceiver in terms of BER and PER. The proposed frequency offset estimator eliminates the frequency offsets effectively and achieves error variance closer to the variance of Cramer Rao Bound. The use of correlation and estimation block instead of de-spreading block improves the error performance of the system. The proposed system less power due to less number of re-transmission caused by packet error. We have proposed complete system architecture and simulated it into MATLAB. This work can be



extended to propose a single system-on-chip including ECG acquisition system and proposed transceiver.

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