SONALI DULANGE

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EDUCATIONAL QUALIFICATIONS

Course/Examination	Institution/University	Year of Passing	CGPA/Marks
MTech Micro-Electronics & VLSI	Indian Institute of Technology, Hyderabad	2022	9.54
B.E. Electronics and Telecommunication	University of Mumbai	2020	9.15
12^{th} (HSC) – Maharashtra State Board	P.E.S. Junior College	2016	78%
10^{th} – CBSE	D.A.V Public School, Airoli	2014	95.8%

Currently pursuing MTech, First year.

SKILLS

Tools – Vivado, Xilinx ISE, Cadence-Virtuoso and Ansys-Lumerical.
Languages – Programming – C, MATLAB, Python; HDL- Verilog, VHDL.
Simulation Software – Spice, Proteus
Database- MySQL
Others- Eagle, STM32, LaTeX

RELEVANT COURSES

Digital Domain – Digital IC Design, Introduction to VLSI Design and Systems Design.
Analog Domain - Analog IC Design, RFIC for wireless communication and Mixed Signal.
Devices and Technology – Semiconductor Device Modelling, VLSI Technology, Nanophotonics and Nanoelectronics.

PROJECTS

- **Simulation of Dipole emission at Exceptional point in a PT-symmetric Cavity** **[January -April 2021]**
  - Simulated Forward and Backward Reflection in PT-symmetric cavity on Ansys-Lumerical to get unidirectional invisibility.
  - Implementing balanced gain-loss PT-symmetric cavity and studying the Purcell effect at different positions.
- **Design of Spiral Inductor using ASITIC** **[March 2021]**
  - Designed L-match network for impedance transformation. Inductor was designed using ASITIC Tool.
  - Minimized Insertion Loss and obtained high Quality factor as well as large SFR using Octagonal spiral.
- **Verilog based project** **[January 2021]**
  - Implemented ADAPTO(Adder-based Dynamic Architecture for Processing Tailored Operators)architecture using Verilog.
  - Verified the Architecture using testbench.
- **Study of Resonant Cavity Enhanced (RCE) Photodetector** **[November – December 2020]**
  - Studied RCE structure, wavelength selectivity and high-speed properties of RCE photodetector, material requirement for RCE photodetector and RCE Quantum Dot Infrared Photodetector.
- **Designing of Node for Wireless Sensor Network (WSN)** **[January 2019 – March 2020]**
  - Designed Embedded system device which is low cost and has efficient energy consumption for WSN application.
  - Implemented device on double sided PCB containing microcontroller, sensor array, transceiver, battery and solar panel.
- **Python based Projects** **[October – November 2018]**
  - Number Recognition- Coded an image-processing based python module to identify a given number, trained the module and tested with varied data set.
  - Space Invaders -Developed a classic arcade game. Designed using Turtle Module in Python.
- **Other Projects**
  - Electronic voting machine using 8051 Microcontroller, Implemented SPI protocol using STM32 and Designed GUI to find Gray level Co-occurrence Matrix by image processing in MATLAB.

TRAININGS

CDAC(Mumbai) – Python Certification
CoreEL Technologies – Design, Implementation and Verification in VLSI
IIRS-ISRO – Satellite Photogrammetry and its Application
NIELIT, Calicut (MEITY) – IEP on FPGA Based Embedded Systems.

INTERNSHIP

- **Bhabha Atomic Research Centre (BARC, Mumbai) Project Trainee** **[December 2018-January2019]**

Analyzed Organic Silicon solar cell, fabricated organic solar cell and computed efficiency, performed gas sensors testing, assisted in fabrication of Thermoelectric Devices and learned about XRD, Mass spectrometer and cryogenic system at BARC.

- **VESIT Internship Program** **[June-July2017 and Dec2017-Jan-2018]**

Developed a Class attendance Mobile app using Android Studio. It is developed to make attendance system paper-free and easily accessible. Worked on RFID based Asset Management System.

CO-CURRICURAL ACTIVITIES

- Participated in Swadeshi Microprocessor Challenge organized by Ministry of Electronics and Information Technology (MEITY).
- Third runner up in poster competition - TECHNOVATION'20
- Represented College at Zonal Level in Aavishkar Project Competition organized by University of Mumbai.
- Attended Regional Mentoring Sessions for Proof of Concept organizes by MHRD's Innovation Cell.

EXTRA-CURRICULAR ACTIVITIES

- Assisted in the development of www.sampoornasez.com and www.jetarc.in using WordPress.
- International Global Volunteer(iGV) at AIESEC in Navi Mumbai.
- Actively participated in Sport Events and Photography events.