

# Pravesh Rathee

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## Technical skills

- **EDA Tools:** Xilinx Vivado, Xilinx ISE, Synopsys DC , IC Compiler ,Cadence Virtuoso , Virtuoso Layout Editor
- **Programming:** Verilog , VHDL ,Basic C
- **Development Kits:** icoboard FPGA iCE40,Digilent ZedBoard Zynq®-7000 ARM/FPGA SoC
- **Basic Knowledge:** Convolutional Neural Network
- Working experience with **Raspberry Pi, Arduino**

## Areas of Interest

- Digital IC Design and Verification, Physical Design ,ASIC and FPGA based design,SoC based design, CMOS based design.

## Education

### Academic Qualifications.....

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| ○ <b>Indian Institute of Technology, Hyderabad</b><br><i>M.Tech in Micro electronics and VLSI , CGPA, <b>8.86/10</b></i>       | <b>Hyderabad</b><br><i>2017-present</i>    |
| ○ <b>UIET , Kurukshetra University</b><br><i>BTech in Electronics and Communication Engineering , Percentage, <b>63.33</b></i> | <b>Kurukshetra</b><br><i>2012-2016</i>     |
| ○ <b>CRPF Public School</b><br><i>Central Board of Secondary Examination, Percentage, <b>80.2</b></i>                          | <b>New Delhi</b><br><i>2011-2012</i>       |
| ○ <b>CRPF Public School</b><br><i>Central Board of Secondary Examination, CGPA, <b>9.2</b></i>                                 | <b>Secunderabad,AP</b><br><i>2009-2010</i> |

### Academic Projects.....

- Worked on hardware-software based re-configurable design of CNN
- Design and simulated the architecture for reconfigurable FFT.
- Design and synthesized 16- bit CORDIC hardware.
- Designed and synthesized 16 - bit Vedic multiplier .
- Design, simulation, verification, layout, DRC, LVS and extraction simulation of half adder circuit..

### Relevant Course Work.....

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|---------------------------------|--|
| ○ Digital IC Design*            | ○ Analog IC Design*                    |
| ○ Semiconductor Device Physics* | ○ Embedded Systems and Hardware Design |
| ○ Mixed Signal Circuit Design*  | ○ VLSI Technology and CMOS Fabrication |