ANAGHA NIMBEKAR

Academic Block C, Room No 617,
IIT Hyderabad, Kandi, Sangareddy,
Telangana, India Pin: 502285
Email: animbekar25@gmail.com
Phone No: +91-7507535078

Seeking a position that will utilize my talent to enhance the growth of the organization, to perform at my best on any responsibilities given to me.

EXPERIENCE

PROJECT ASSISTANT, INDIAN INSTITUTE OF TECHNOLOGY, HYDERABAD
JULY 2019
Working on image processing, machine learning, FPGA and DRONE.

TEACHING ASSISTANT, SHRI RAMDEOBABA COLLEGE OF ENGG AND MANAGEMENT, NAGPUR
AUGUST 2017-MARCH 2018
Teached DCFM, Digital signal processing, CMOS.

EDUCATIONAL QUALIFICATIONS

Course	Institution	Board/ university	Passing Year	CGPA/percentage
M.TECH	RCOEM, Nagpur	RTM Nagpur University	2019	7.61 CGPA
BE	SVPCET, Nagpur	RTM Nagpur University	2017	7.26 CGPA
HSC	NK College, Bhandara	MH State Board	2013	59.33%
SSC	NK College, Bhandara	MH State Board	2011	88.91%

Note: Qualified GATE 2017 examination.

PROJECTS

- **DEVELOPMENT OF LOCAL POSITONING SYSTEM USING LOCALITY SENNSITIVE HASHING**
  under the guidance of ***Dr. Amit Acharyya, Dept. of Electrical Engineering, IIT Hyderabad.***
  Duration: August 2018- July 2019
  Description: This project was developed with the aim of navigating a person or device in local area. This project includes image processing, Locality Sensitive Hashing. Worked on OPENCV Python. Worked on PYNQ-Z1, ZCU102, JETSON TX2, JETSON Nano.
- **IMPLEMENTATION OF DIGITAL FILTER ON FPGA.**
  Under the guidance of ***Prof. Sharmik Admane, Dept. of VLSI Design, RCOEM, Nagpur.***
  Duration: January 2018- March 2018
  Description: A digital FIR filter is designed using system generator through MATLAB. Generated its Netlist and implemented it on FPGA using VIVADO.
- **DIGITAL ALARM CLOCK USING VERILOG**
  Under the guidance of ***Dr. Pankaj Joshi, Dept. of VLSI Design, RCOEM, Nagpur.***
  Duration: August 2017- October 2017
  Description: As clock is reset, it starts its count from 00:00:00 and increment at each 1 sec. When the alarm time is reached and buzzer starts. The FPGA we used is of 1MHz clock so to convert it into real-time clock we have implemented the counter circuit.

❖ **OBSTACLE DETECTION AND NAVIGATION SYSTEM FOR VISUALLY IMPAIRED.**

Under the guidance of ***Prof. Faizy, Dept. of Electronics and telecommunication engineering, SVPCET, Nagpur.***
Duration: August 2016- March 2017

Description: This project was developed with an aim to make a system which will be helpful for visually impaired to make them travel independently. It consists of two modules one is pocket module and another is shoe module. Both modules can communicate with the GSM.

❖ **DETECTION OF HUMAN IN THE RANGE OF PASSIVE INFRARED SENSOR (PIR).**

Under the guidance of ***Prof. Binu Joy, Dept. of Electronics and telecommunication engineering, SVPCET, Nagpur.***
Duration: January 2015- March 2016

Description: This project's aim was to make a system which can detect presence of human in the range of the sensor. It can be used in institutes, ATM rooms, houses, etc.

RESEARCH AREA

- Machine learning techniques for Digital Image Processing.
- FPGA for the development of Embedded Systems involved in Signal Processing.

TRAINING & INTERNSHIP

- Project Intern at Indian Institute of Technology, Hyderabad (August 2018- July 2019).
- Completed training on "PCB DESIGN AND MANUFACUTRING" at COPPER TRACK INDUSTRIES, NASHIK.
- Completed vocational training programme at "DOORDARSHAN KENDRA, NAGPUR".

WORKSHOPS & SEMINARS

- Participated in workshop on System Verilog for Verification at RCOEM, NAGPUR.
- Presented paper in "EUPHORIA" at Priyadarshini College of Engineering, Nagpur.
- Participated in workshop on INTRODUCTION TO RASPBERRY PI at SVPCET, NAGPUR.

SKILLS

- Programming : Python, MATLAB, Basics of C & C++, HDL (VHDL & Verilog HDL).
- Software Tools : Vivado, ISE Design Suite, Keil µvision, Questa Sim, Mentor Graphics (Pyxis), Spice, MATLAB,
- Hardware Tools : NVIDIA Jetson TX2, NVIDIA Jetson Nano, PYNQ-Z1, ZCU102, ZED Board, Cortex-M0 FRDM-KL25Z (for Embedded Systems applications), Nexys 4 Artix-7 Board (for digital design applications).

LANGUGES

English	Professional
Marathi, Hindi	Native Speaker
Kannnada	Basic

DECLARATION

I hereby declare that the above mentioned information is correct up to my knowledge and I bear the responsibility for the correctness of the above mentioned particular.
Date: August 19, 2019
Place: Hyderabad

Anagha Nimbekar