SRISUBHA KALANADHABHATTA

Experience: 12 Years

EDUCATION

- Pursuing Ph.D. at IIT Hyderabad from Jan 2015
- M.E., VLSI Systems from N.I.T., Trichy, with 9.2 CGPA during 2001-03.
- B.Tech, Electronics & Communications from J.N.T.U with 86.69% during 1997-2001. University second rank.

PROFILE

- Excellent organizer with solid planning and problem-solving skills.
- Commitment to Continuous learning, skill development, Team work.
- Ability to handle complete FrontEnd Flow

EXPERIENCE

Team Lead, **Red Pine Signals Limited**, Hyderabad from April 2005 till date.
Working in Frontend and Silicon Test.

Member, Technical Staff**, QualCore Logic Limited**, Hyderabad from June 2004 till March 2005.
Worked on ASIC tools, Backend.

Engineer, **Infosys Technologies Limited**, Mysore from April 2003 till May 2004.
Worked on Xilinx FPGAs and CPLDs. Done VHDL Coding and verification.

Project Trainee, in E.C.E. Dept of R.E.C., Trichy for M.I.T. Project from June 02 till Feb 03.

SKILLS

EDA Tools Handled

Synopsys Frontend tools like VCS, DVE, DC, PT, Formality, VSI LP
Mentor Graphics DFT tools like TessentMBIST, Fast Scan and Test Kompress
Cadence Encounter
Xilinx ISE

Platforms and Languages

Verilog
C, Unix, Perl, Tcl, Vi
MS Windows 98/2000/NT/XP

ACHIEVEMENTS

- University **second** ranker in B.Tech (J.N.T.U.) with 86.69%.
- Gold medalist in B.Tech (awarded by college).

PROJECTS HANDLED

RTL to Netlist -- Complete Frontend Flow

The flow for complete Frontend starting from chip Synthesis to delivering the netlist to backend is handled by me. This includes

1. Chip integration of the digital and analog blocks and making the final RTL, relevant checks on the RTL. Test Mode architecture is also part of this.
2. Pad Order and Packaging
3. DFT Insertion for MBIST and BSCAN
4. Synthesis
5. VSI LP, MVRC
6. Formality
7. Power Analysis
8. ATPG

Silicon Test

This includes creating the test methodology and working with the tester house for achieving the required Yield on the Silicon.