UTKALIKA PANDA

Current location:
Hyderabad

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CAREER OBJECTIVE:

To work in a creative and challenging environment, where my knowledge can be shared and enriched, resulting in growth of the organization as well as personal skill enhancement.

EDUCATIONAL PROFILE:

Degree	Institute	Year	%/CGPA
M. Tech [Microelectronics and Vlsi]	Indian Institute of Technology, Hyderabad	2014	8.48
B. Tech (ECE)	Krupajal Engineering College, Bhubaneswar	2010	7.84

AREA OF INTREREST:

- Digital VLSI Architecture Design and complete backend flow for ASIC Implementation.
- Interested in EDA and CHIP Design.
- Analog IC Design

TECHNICAL SKILLS:

- **Programming Languages** C, C++, Verilog, VHDL, 8085 & 8051 Assembly programming**,** Basic shell scripting.
- **Tools**: ModelSim Simulator, RTL Compiler, Xilinx ISE(Virtex-7 and Spartan-6) , ,DC Formality, ICC, MATLAB , Cadence Virtuoso , VCS, Cadence HAL , Latex.
- **Training** Attained training on Symphony C Compiler, Design Compiler, and IC Compiler at Synopsys Hyderabad .

- **Operating System & Microcontroller** Windows XP, Windows 2007, LINUX, ARM Cortex – M3

COURSES TAKEN AT IITH:

- VLSI Technology.
- Semiconductor Devices and Modeling
- Digital IC Design
- Analog IC Design
- Embedded Systems
- Biomedical IC Design
- Digital Signal Processing

SIGNIFICANT PROJECT PROFILE:

M.TECH :-

Title : ***FPGA Prototype and ASIC Implementation of Low Complex and Low power Architecture Design*** *for Reduced 3-Lead to Standard 12 Lead ECG Signal Reconstruction* ***architecture*** *for Remote Health Care Monitoring.*

Description : Aim of this project is to replace the decade old bulky state of art ECG machine (comprise of 10 electrode and 12-lead signals) by a cheap and affordable product . More precisely reconstructing the state of art 12 lead signal from the reduced 3-lead signal which will ease the patient and doctor's flexibility to check the heart condition . To bridge the gap between our already proposed algorithm and architecture this project come up with a very low complex and low power architecture and its FPGA prototype and ASIC implementation which will open up a significant opportunity in remote health monitoring system development and will help making the concept of personalized healthcare a reality.

B.TECH :-

Title : ***Wireless Traffic Jam Controller using Microcontroller***
Role : TEAM MEMBER.

Description : Aim of the project is to design traffic jam detector and control system which will be transmitted to control room to indicate traffic jam route in wireless method & also broadcast through a FM transmitter by a traffic police so that other traffics approaching the point will divert their vehicle to other route .Transmission of signal to the control room is done by radio waves using ASK digital data transmission.

Summer Training : Done training on RF Optimization arranged By BSNL in Bhubaneswar .

Publication:

Panda, Utkalika; Maheshwari, Sidharth; Padma, Gayathri; Thendral, Murugaiyan; Acharyya, Amit; Puddu Paolo Emilio; Schiariti, Michele, "**Personalised System-on-chip for Standard 12-lead Reconstruction from the Reduced 3-lead System Targeting Remote Health Care**," Computing in Cardiology 2014 (Accepted)

WORK EXPERIENCE:

- Company : Suddhananda engineering and Research Center, Bhubaneswar
- Duration : 2010 – 2012
- Role : Lecturer
- Responsibility : Conducted lectures on Basic electronics, Digital electronics & Signals and systems

STRENGTHS:

- Good learner, Flexible and hardworking.
- The ability & interest to learn new scientific tools.
- Good initiative and having ability to deal with colleagues professionally.

HOBBIESs:

- Playing Badminton.
- Swimming
- Listening to music

DECLARATION:

I here by declare that all the information furnished above is true and correct to the best of my knowledge and belief.

(Utkalika Panda)