Ramyalakshmi K Gunukula

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OBJECTIVE

To put in my best efforts to achieve the goals of the organization.

SUMMARY

- Good understanding of the ASIC and FPGA design flow.
- Experience in writing RTL models in VHDL and Verilog HDL and Testbenches in SystemVerilog.
- Experience in using industry standard EDA tools for the front-end design and verification.
- More than 1 & ½ year of experience in the Design Verification projects.

VLSI Domain Skills

HDL	:	Vhdl, Verilog
HVL	:	SystemVerilog
Verification Methodologies	:	Coverage Driven Verification,OVM
EDA Tool	:	Modelsim and ISE.
Domain	:	ASIC/FPGA Design Flow, Digital Design methodologies
Knowledge	:	RTL Coding, FSM based design, Simulation, Code Coverage, Functional coverage

EXPERIENCE

Project Assistant : Indian Institute of Technology, Hyderabad, India(July 2014 –To present)

FPGA Design Engineer : Arks Microelectronics India Pvt. Ltd, Hyderabad, India(Nov 2013 –Jun 2014)

VLSI Verification Intern : Aadi Semicon solutions Pvt. Limited, Bangalore, India (Jan 2013 – NOV 2013)

Maven Silicon Certified Advanced VLSI Design and Verification course
From Maven Silicon VLSI Design and Training Center, Bangalore.
June 2012 – November 2012

PROJECTS

Project:1

Currently **working** on A Low-Complexity ECG Feature Extraction Algorithm for Mobile Healthcare Applications.
Description : A low-complexity algorithm for the extraction of the fiducial points from the Electrocardiogram (ECG). The application area we consider is that of remote cardiovascular monitoring, where continuous sensing and processing takes place in low-power, computationally constrained devices, thus the power consumption and complexity of the processing algorithms should remain at a minimum level. Under this context, we choose to employ the Discrete Wavelet Transform (DWT) with the Haar function being the mother wavelet, as our principal analysis method.

Project:2

worked on 7 segment display using CPLD.
Role :RTL coding ,interfacing hardware circuit needed for Spartan-3 kit to get desired output as per the requirement.
EDA Tools : Xilinx 10.1

Description :with the input of 10Mhz,desired clock is derived using decade counter.Time is generated n displayed using 7 segment display decoder..n still working on this project.

Project:3

UART –Universal Asynchronous Receiver Transmitter(Design)

Role : RTL coding, simulation and sythesis

EDA Tools : Xilinx 10.1

Description : A UART (Universal Asynchronous Receiver/Transmitter) is the microchip with programming that controls a computer's interface to its attached serial devices. Specifically, it provides the computer with the RS-232C Data Terminal Equipment (DTE) interface so that it can "talk" to and exchange data with modems and other serial devices.

1) Architected the design and described the functionality using VHDL
2)Verified the RTL model.
3) Synthesized the design.

Project:4

Router 1x3 – RTL design and Verification

Description :

The router accepts data packets on a single 8-bit port called data and routes the packets to one of the three output channels, channel0, channel1 and channel2.

Team size : 2

Role : RTL coding, simulation and synthesis

EDA Tools: Modelsim, Questa – Verification Platform and ISE

Architected the design and described the functionality using Verilog HDL.

Verifying the RTL model using System Verilog

EDUCATION

- **SSC(2005-06)**
  HOC International School & Junior college,Rasayani
  Maharashtra State Board,76.40%

- **HSC(2007-08)**
  HOC International School & Junior college,Rasayani
  Maharashtra State Board,82.50%

- **B.TECH in Electronics & Tele-Communication Engineering, *Dr.Babasaheb Ambedkar Technological University,2012*.**
  August 2008 – June 2012.
  Cumulative Grade Point Average (CGPA) = 6.77

B.Tech Project (July 2011-June 2012)

Garbage compaction

Description:

waste compaction is the process of compacting waste. Compaction means to compress, condense or consolidate. It is often used to reduce the size of waste material. Garbage compactors and waste collection vehicles compress waste so that more of it can be stored in the same space. Waste is compacted again, more thoroughly, at the landfill to conserve valuable airspace and to extend the landfills life span. The purpose of this project is to implement the various concepts of microcontroller and embedded designing environment.

Team size : 3

Role : Hardware designing and coding using assembly language program.

PRESENTATIONS

Participated in National level paper presentation, technical event,cynosure-2011 held in our university.

Declaration

I hereby declare that all information mentioned above is true to the best of my knowledge.

Date:

(RAMYALAKSHMI GUNUKULA)