Curriculum Vitae

Basireddy Karunakar Reddy
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Indian Institute of Technology Hyderabad
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EDUCATIONAL QUALIFICATIONS

Qualification	**University/ Board**	**Duration**	**Percentage/Grade of Marks**
M.Tech (Pursuing-Microelectronics & VLSI)	Indian Institute of Technology Hyderabad	2012-2015	9.52/10 (1st year)
B.Tech (ECE)	Yogi Vemana University	2008-2012	9/10
Intermediate (MPC)	Board of Intermediate Education	2006-2008	97.1%
X class (SSC)	Board of Secondary Education	2005-2006	88.5%

HARDWARE/SOFTWARE SKILLS

S/W or H/W Languages : C, VHDL
Scripting languages : Perl, C-shell
Platforms : Linux, Windows.
Tools (CAD) : Modelsim, Xilinx ISE, synphony C compiler, Design Compiler, IC Compiler, Cadence Virtuoso, SILVACO TCAD.

B. Tech THESIS:

Design and implementation of radix-4 based high speed multiplier for ALU's using minimal partial products. It reduces the number of partial products and power using booth algorithm.

ACHIEVEMENTS & CO-CURRICULAR ACTIVITIES:

- Scored highest CGPA of 9.52 out of 10 in M.Tech (1st year, VLSI), EE, IIT Hyderabad.
- Received national merit scholarship from government of India.
- Ranked 2nd among all in the university during B.Tech, ECE.
- Scored highest mark in the district 971/1000 in 12th standard (Maths-297/300, physics-116/120, chemistry-119/120).
- Got many prizes in various sports events in school and college level.

PERSONAL DETAILS

Date of Birth	: 01-07-1991
Gender	: Male
Nationality	: Indian
Languages Known	: English, Hindi, and Telugu.
Hobbies	: Reading books, listening music, and playing Cricket.

PUBLICATIONS

B.Karunakar Reddy, Srinivas Sabbavarapu, Amit Acharyya, "A New VLSI IC Design Automation Methodology with Reduced NRE Costs and Time-to-Market using the NPN class Representation and Functional Symmetry", IEEE International Symposium on Circuits and Systems (ISCAS),Australia, 1-5 June,2014 (Accepted).

Pramod Kaddi, **B. Karunakar Reddy**, Shiv Govind Singh, "Active Cooling Technique for Efficient Heat Mitigation in 3D-ICs"IEEE 27th International Conference on VLSI Design, IIT Bombay, 5-9 January, 2014, pp.495-498.

B.Karunakar Reddy, S. Sabbavarapu, K. Gupta, R. Prabhat, A. Acharyya, R. A. Shafik and J. Mathew (2013), "A Novel and Unified Digital IC Design and Automation Methodology with Reduced NRE Cost and Time-to-Market", *IEEE International Symposium on Electronic System Design*, Singapore, 12-13 December, 2013,pp. 36-40.

S. Sabbavarapu, **B.Karunakar Reddy**, R. Prabhat, K. Gupta, A. Acharyya, R. A. Shafik and J. Mathew (2013), "A Novel Physical Synthesis Methodology in the VLSI Design Automation by Introducing Dynamic Library Concept", *IEEE International Symposium on Electronic System Design*, Singapore, 12-13 December, 2013, pp. 103-107.