Contact

vcs.srinivas@gmail.com

www.linkedin.com/in/chandrasekhara-s-vatti-3bb0b419 (LinkedIn)
www.broadcom.com (Company)

Top Skills

ASIC
Verilog
Integrated Circuit Design

Languages

English (Professional Working)
Telugu (Native or Bilingual)
Hindi (Full Professional)

Publications

A VLSI system-on-a-chip (SoC) for digital communications

Chandrasekhara S Vatti

Principal Engineer
Hyderabad, Telangana, India

Summary

A versatile design engineer with experience in different ASIC design methodologies from requirements to production. Specific strengths in High-speed digital design, Synthesis, STA, Timing closure and Verification with good hands on experience in DMA and hardware security blocks. Ability to Lead and work in cross-functional design teams.

Experience

Broadcom
11 years 5 months

Principal Engineer - IC Design
March 2015 - Present (5 years)

RTL design and verification of high speed peripherals like DMA engines for DSL chips

Sr. Staff Engineer
March 2011 - February 2015 (4 years)

RTL design and verification of high speed peripherals like DMA engines for DSL chips

Staff Engineer-II
October 2008 - February 2011 (2 years 5 months)

RTL design and verification for DSL chips

Advanced Micro Devices
Senior Engineer
October 2006 - September 2008 (2 years)

RTL design and verification of DTV chips

Defence Research and Development Organisation
Scientist C
March 2003 - September 2006 (3 years 7 months)

RTL design and verification of Sat. Com receiver chips

Education

Indian Institute of Technology, Hyderabad

Doctor of Philosophy - PhD, Machine Learning in HW Security and Fault Tolerant VLSI design · (2019 - 2023)

Birla Institute of Technology and Science

M.E, Micro Electronics · (2010 - 2012)

National Institute of Technology Warangal

B.Tech, ECE · (1998 - 2002)

Sir C R Reddy Polytechnic

Diploma in Electronics & Communicaton Engineering, Electronics & Communication · (1995 - 1998)